Technical Data
Multiuse Programmable
Serial Interface

For HP 1000 A–Series Computer Systems
Product Number
12043A
Features

- Z–80A CPU microprocessor control
- One Z–80A SIO/2 dual–channel serial I/O ▒USART▒ controller
- Full– or half–duplex mode
- Synchronous or asynchronous features
- CRC–16 or CCITT block frame check for synchronous operation
- Two modem control inputs and two modem control outputs per channel
- Optional vectored interrupts per channel
- Capability for two independent RS–232–C primary channels
- Two Z–80A DMA direct memory access controllers
- 16 Kbytes of Dynamic RAM for tables, buffers, and/or firmware
- One Z–80A Counter Timer Chip providing one system timer, an independent, programmable baud rate for each SIO channel, and a programmable DMA backplane transfer rate.
- Capability for EIA RS–449, EIA RS–232–C
- Multidrop capability
- Internal loopback of clocks and transmitted data under firmware control for self–test
- Four programmable indicator lights (LEDs)
- Eight switches, accessible as a single byte
- EPROM–based developmental debug monitor
- EPROM–based self–test
- Off–line RAM dump to host
- EPROM–based program for loading and executing downloaded code
- HP support

Functional Description

The HP 12043A is a microprogrammable interface for the HP 1000 A–Series Computer System. This card is intended to be purchased by customers who will use it with HP software downloading the characterizing protocol into 16 Kbytes of on–card RAM memory. The HP 12043A executes Multileaving Remote Job Entry protocol. Because the interface program is downloaded from software into RAM memory on the card, the interface never needs to be modified by the addition of EPROMs. This means the 12043A is used and supported as shipped from the factory. An 8 K EPROM on each interface contains programs for self–test, loading and executing code, and a development and debug monitor. The card is configurable through software.

Onboard Microprocessor Offloads Host Computer

A powerful microprocessor on the interface manages routine communications processing, relieving the host computer for applications–oriented tasks. Under control of downloaded firmware, the microprocessor converts command words into actions, such as establishing a communications link or loading/unloading data from the onboard buffers to the host CPU. The microprocessor can also perform protocol generation and interpretation, error checking, error recovery by retransmission, or general purpose I/O interfacing, all without the attention of the host computer.

16 Kbytes of RAM

Onboard memory allows messages and associated information to be buffered on the card either for transmission, reception, or temporary program storage. Thus, interrupts to the host processor can be kept at a minimum so the host CPU can be put to better use processing applications.

Direct Memory Access Transfers

Each interface card has its own DMA intelligence to control transfers of data between the card buffer and the host CPU backplane. DMA reduces the time and overhead required to move messages between interface and host CPU memory.

EPROM–based Self–Tests

A go/no–go self–test, performed at power–up or reset of card, helps to ensure reliable operation of the interfaces and minimize troubleshooting time. These tests check out the RAM memory, the

Direct Memory Access operations, baud rate generators, and the I/O parts of the communication interface and signal self–tests results via LED indicators. The self–test can also be run with the supplied diagnostic hood. The diagnostic hood fits on the edge of the PSI card and tests more of the card than is possible with self–test alone.

EPROM–based Developmental Debug Monitor (DDM)

The DDM program serves as a monitor to aid in the development of user firmware. Once a firmware program is cross–assembled on a minicartridge tape, the DDM can load that program into the PSI card's RAM through an HP 2645 or 2648 terminal and a terminal–to–card–to–link cable supplied with the DDM. The DDM can then support these functions:

- Display and/or modification of memory locations
- Display and/or modification of registers
- Control of program flow by:

a. transferring control to firmware entry points,
b. setting and removing break points,
c. single–step simulation with trace

- Reading and writing through all I/O ports
- Creating (punching) modified code into 264x minicartridge tape
- Help facility providing information about the command set

Functional Specifications

Transmission Mode
Full or half duplex, bit–serial, synchronous or asynchronous

Z–80A SIO/2 Characteristics
Data Buffering: Received data quadruple buffered; transmitted data double buffered

Synchronous Features for Character Oriented Protocol:
- 1 or 2 Sync characters
- Automatic Sync character insertion
- Cyclic redundancy check generation and checking
- Received data overrun detection

Synchronous Features for Bit Oriented Protocol:
- Abort sequence generation and checking
- Automatic Zero insertion and detection
- Automatic Flag insertion between messages
- Address field recognition
- Supports 1 to 8 bits per channel
- Cyclic redundancy check generation and checking
- Valid receive message overrun detection

Asynchronous Features:
- 5, 6, 7, or 8 bits per character
- 1, 1–1/2, or 2 stop bits
- Even, odd, or no parity
- X1, X16, X32, or X64 clock modes
- Break generation and detection
- Parity, overrun, and framing error detection

Optional Generation of a Vectored Interrupt per Channel when:

- The state of an SIO modem control input changes
- The transmit buffer is empty
- A receive character is available
- A special receive condition occurs for: parity error, Rx overrun error, CRC/Framing error, End of Frame

Z–80A DMA Characteristics

Three Classes of Operation: Transfer only, Search only, Search and Transfer.

Three Modes of Operation: Byte–at–a–time, Burst (continuous as long as both sides are ready), Continuous (locks out CPU until done). Read and Write port addresses can independently increment, decrement, or stay fixed.

Interrupts: On Match Found, End of Block, or Port Ready. Each can be its own interrupt vector.

Address and Block Length Register Loading: Registers may be loaded for the next operation without disturbing current operation.

Operation Restart: Last operation can be restarted automatically or on command.

DMA Signaling: DMA can signal when a specified number of bytes have been transferred without disturbing the current system.

DMA Status: CPU can read the current channel status, Read or Write address registers or the length register.

Z–80A Counter Timer Chip Characteristics

Channels: Four independently programmed channels, used for dynamic RAM timing, Zilog–chip main–system clock and baud rate generator for each SIO channel.

Baud rate limits are:
Asynchronous: max 57.6 K,min 50 **Synchronous**: max 460.8 K,min 50
Synchronous External: max 810 K

Note: The speed of transmission depends on and may be limited by the type of firmware protocol implemented. The best practical board rates that can be expected with sophisticated protocols are 230 Kbaud synchronous and 57.6 Kbaud asynchronous.

Modes: Operates in Counter or Timer mode.

Interrupt: On the zero count condition (each channel has its own interrupt vector).

Restart: Automatically restarts the last operation in either mode.

Output: Gives the Z–80A CPU the number of counts to go until a zero count condition.

Communications Interface Characteristics

Number of Input Lines: Six input lines with balanced receivers and eight input lines with unbalanced receivers

Output Lines: Four output lines that can be driven by unbalanced or balanced line drivers, eight output lines with unbalanced line drivers

Configuration Information

Computer I/O Channels Required: One per interface

Interface Current Required from Computer Power Supplies:

+ 5 V Supply	+12 V Supply	−12 V Supply
2.60 A	0.35 A	0.18 A

Compatible Modems: The HP 12043A interface is compatible with the modems listed below and may be useful with other modems that are compatible with both the PSI card hardware and user−developed firmware. Note that compatibility with any modem is highly dependent on the firmware implemented on the PSI card.

Connections and Compatible Modems

Connection via Private Lines:

- Bell 201C
- Bell 208A
- Bell 208B
- Bell 209A

System Compatibility:

PSI Card System Compatibility

	Compatible Computer	Compatible Computers	Systems
2137A	2196C/D		
2139A	2197C/D		
2156B	2199C/D		
2436A/E	2486A		
2437A	2487A		
2439A	2489A		

Ordering Information

The HP 12043A includes:

12043–60001 Modem Programmable Serial Interface Assembly; includes 5180–1966 Self–Test/Download EPROM
5061–4914 5–meter (18 ft) RS–232–C Modem Interface Cable
5061–4916 Self–Test Hood
5955–7700 Installation and Reference Manual

HP 12043A Option

001 5061–4993 5–meter (18 ft) RS–449 Modem Interface Cable (delete 5061–4914)